WHAT IS CLAIMED IS:

1. A method of growing a semiconductor layer in a selective area by MOCVD (Metal Organic Chemical Vapor Deposition), comprising the steps of:

(a) forming a first mask pattern on a semiconductor substrate having a (100) crystalline plane, said first mask pattern having a first window wider than the selective area;

(b) forming a second mask pattern having both a second window and a third window, the second window being defined by spacing of the second mask pattern from the first mask pattern, in correspondence with a blocking area for blocking the surface migration of a III-group semiconductor source gases at edges of the first window, and the third window being as wide as the selective area; and

(c) growing the semiconductor layer by MOCVD on the semiconductor substrate exposed by the second and third windows.

2. The method of claim 1, wherein the first and second mask patterns and the first, second and third windows are formed in parallel to the (100) crystalline plane of the semiconductor substrate.

3. The method of claim 2, wherein step (b) includes forming the second mask pattern such that at least one pair of second windows are defined, for forming at least one pair of blocking areas, and the thickness of the semiconductor layer grown in the selective

area is controlled by adjusting a number or width of the second windows.

4. The method of claim 1, wherein the semiconductor layer grown in the selective area is an active layer for an SSC-LD (Spot-Size Converter integrated Laser Diode).

5. The method of claim 1, wherein the semiconductor layer grown in the selective area is formed of AlGaInAs.

6. The method of claim 1, further comprising the step of forming a trench by etching the semiconductor substrate exposed by the second window.

7. A method of growing a semiconductor layer in a selective area by MOCVD (Metal Organic Chemical Vapor Deposition), comprising the steps of:

(a) forming a first mask pattern, on a semiconductor substrate having a (100) crystalline plane, said first mask pattern having a first window being wider than the selective area;

(b) forming a second mask pattern having at least one second window and a third window, the second window being defined by spacing the second mask pattern from the first mask pattern, in correspondence with a blocking area for blocking the surface migration of III-group semiconductor source gases at edges of the first window, and the third window being as wide as the selective area;

(c) forming at least one trench by etching the semiconductor substrate exposed by the second window; and

(d) growing the semiconductor layer by MOCVD on the semiconductor substrate exposed by the third window and the trench.

8. The method of claim 7, wherein both the first and second mask patterns and the first, second and third windows are formed in parallel to the (100) crystalline plane of the semiconductor substrate.

9. The method of claim 7, wherein the thickness of the semiconductor layer grown in the selective area is controlled by adjusting a number, width or depth of trenches.

10. The method of claim 7, wherein the trench is formed into the shape of a reverse mesa or a square.

11. A SiO_2 mask pattern for a Spot Sized Converter Integrated Laser Diode (SSC-LD), comprising:

an InP substrate having a (100) crystalline plane;

a first pair of mask patterns comprising a two mask patterns arranged on opposite ends of the InP substrate with a central window there between;

a second pair of mask patterns arranged between the first pair of mask patterns arranged on opposite ends of the InP substrate, each mask of the second pair being arranged

adjacent a respective first mask pattern;

a third pair of mask patterns, each one third mask pattern of said pair being arranged between a respective one of a second pair of mask patterns and a respective one of a first pair of mask patterns;

wherein a second pair of windows comprises a first gases migration blocking area (MBA) that is formed between each respective second mask pattern and a third mask pattern; and

wherein a third pair of windows comprises a second gases migration blocking area (MBA) that is formed between each respective first mark pattern and third mark pattern.

12. The mask pattern according to claim 11, further comprising semiconductor growth layers being formed in the MBAs of the second window and third window.

13. The mask pattern according to claim 12, further comprising a semiconductor layer arranged in the central window.

14. The mask pattern according to claim 13, wherein the semiconductor layer grown in the central window is an active layer for an SSC-LD.

15. The mask pattern according to claim 11, wherein both the first and second mask patterns and the central, second and third windows are formed in parallel to the (100) crystalline plane of the semiconductor substrate.

16. The mask pattern according to claim 13, further comprising trenches that are formed into the first and second MBAs, said trenches being formed in the InP substrate.

17. The mask pattern according to claim 16, further comprising growth layers that are formed respectively in the trenches that extend beyond a surface of the InP substrate.